## REMARKS

Favorable reconsideration and allowance of the claims of the present application are respectfully requested.

In view of the telephonic election of Group I, Claims 1-11, that was made with applicants' representative on July 13, 2004, applicants hereby affirm that election to prosecute Group I, Claims 1-11. Accordingly, Claims 1-11 are pending and Claims 12-18 have been withdrawn by the Examiner as being directed to a non-elected invention.

Before addressing the specific grounds of rejection raised in the present Office Action, applicants have amended Claim 1. Specifically, applicants have amended Claim 1 to positively recite that the trimming the at least one patterned hard mask in said FinFET region provides a trimmed patterned hard mask in the FinFET region that has a horizontal surface whose width is less than that of each of the patterned hard masks in the FET region. Support for this amendment to Claim 1 is found in paragraph [0050] and FIG. 7.

Applicants note that the trimmed patterned hard mask in the FinFET region provides a FinFET that is double gated, while the patterned hard mask in the FET region provides a single gated device.

Since the above amendment to Claim 1 does not introduce new matter into the specification of the instant application, entry thereof is respectfully requested.

Claims 1-4, 5, 7, 9 and 11 stand rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of U.S. Patent No. 6,252,284 to Muller, et al. ("Muller, et al.") and U.S. Patent No. 6,166,413 to Ono ("Ono"). Claims 6, 8 and 10 stand rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined

disclosures of Muller, et al., Ono and U.S. Patent No. 6,657,259 to Fried, et al. ("Fried, et al.").

Applicants respectfully submit that the method of the present invention, as recited in Claims 1-11, is not rendered unpatentable by the combined disclosures of Muller, et al., Ono and Fried, et al. Specifically, the combined prior art references do not teach or suggest a method that forms a FinFET device and a FET device wherein the FinFET device is perpendicular to the FET device using the claimed processing steps. Specifically, the applied references do not teach or suggest a method which includes, among other steps, a step of trimming at least one patterned hard mask in a FinFET region, wherein each trimmed patterned hard mask in said FinFET region has a horizontal surface whose width is less than the width of that of each patterned hard mask in said FET region.

The principal reference spurring each of the obviousness rejections, i.e., Muller, et al., is defective since the prior art method does not teach or suggest a method of forming a FinFET device and a FET device in which the FinFET device is perpendicular to the FET device using among other steps applicants' claimed trimming step. Muller, et al. provide a method of making an improved Fin device which is useful in forming a FinFET. The principal reference does not teach or suggest that the disclosed process can be used to integrate a FET device with the FinFET device. Applicants further observe that in Muller, et al, a trimmed hardmask is used in making the FinFET device but there is no teaching or suggestion of its relationship to the patterned hard masks that are used in forming a FET device. Indeed, Muller, et al. do not mention that their disclosed process can also be used in fabricating a FET device, as presently claimed. Moreover, since

Muller, et al. do not teach or suggest the presence of a FET device, the applied reference does not teach or suggest the claimed feature that the FinFET active device region (and hence the resultant FinFET device) is perpendicular to the FET active device region (and hence the resultant FET device).

Ono does not alleviate the above defects in Muller, et al. since the applied secondary reference does not teach or suggest a method of forming a FinFET device that is perpendicular to the FET device using the claimed trimming step in which each trimmed patterned hard mask in said FinFET region has a horizontal surface whose width is less than the width of that of each patterned hard mask in said FET region. Ono provides a method of fabricating a n-channel type FET and a p-channel type FET in which separate block masks are used. The applied secondary reference does not teach or suggest applicants' claimed method that results in FinFET device that is perpendicular to the FET device in which the claimed trimming step is used. As such, the combined disclosures of Muller, et al. and Ono do not render the claimed method obvious.

Fried, et al. do not alleviate the above defects in the combined disclosures of Muller, et al. and Ono since it also does not teach or suggest a method of forming a FinFET that is perpendicular to a FET using the claimed trimming step that defines the FinFET and FET regions. Fried, et al. provide a method of forming FinFETS on the same substrate utilizing various crystal planes for FET current channels in order to optimize mobility and/or reduce mobility. Applicants observe that the method disclosed in Fried, et al. pertains to FinFET devices only, and there is no teaching or suggestion that the disclosed process can also be used to form a FET.

As such, the combined disclosures of Muller, et al., Ono and Fried, et al. do not render the claimed method obvious.

The § 103 rejections also fail because there is no motivation in the prior art that suggests modifying the disclosed methods to provide a FinFET that is perpendicular to a FET in which the claimed trimming step is used to define the active areas for both the FinFET and FET regions. Muller, et al. and Fried, et al. are concerned with providing FinFET devices only. Ono provides FET devices only. The combination does not provide a method that includes applicants' claimed trimming step which defines the FinFET region and the FET region. Thus, there is no motivation provided in the applied reference, or otherwise of record, to make the modification mentioned above. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." *In re Vaeck*, 947 F.2d, 488, 493, 20 USPQ 2d. 1438, 1442 (Fed.Cir. 1991).

The rejections under 35 U.S.C. § 103 have been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

Wherefore, consideration and allowance of the claims of the present application are respectfully requested.

Respectfully submitted,

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